IMSAI Series II

External Architecture Specification

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1. Introduction

The next evolution of the original **IMSAI 8080** offers outstanding features and capabilities for hobbyists, students, software and system developers, and anyone else wishing to develop 8-bit applications and hardware. The IMSAI Series Two retains the "look and feel" of the original IMSAI 8080 but adds functionality and performance that greatly surpass its predecessor.

The IMSAI Series Two is comprised of the following components:

Chassis modeled after the original **IMSAI 8080**, utilizing the same aluminum construction, familiar switch-and-LED layout, color, and finish as its predecessor.

350 watt PC-ATX style power supply standard, 400 and 500 watt capacity available as an option.

Power supply booster module which provides the +16, -16, and +8 voltages required by the IEEE-696 Bus.

EXP-9/AT - 9-Slot terminated IEEE-696 backplane.

MPU-C Processor Board containing Zilog Z8S180 CPU, 1MB SRAM, 128K FLASH, and provision for an 8/16/32K EPROM, two serial ports, and a Z8S180 localbus to IEEE-696 bridge.

Super-I/O Board which provides a dual floppy interface, dual channel IDE disk interface, two RS-232 serial ports with modem control, parallel port, real-time-clock, and PS/2 keyboard and mouse ports.

Provision for mounting an internal ATX-style motherboard system, and support for serial and parallel port interface between platforms, hardware and software switching capability between the operating platforms for the keyboard; essentially two systems in one enclosure

System and software support available for CP/M and ZS-DOS

IMSAI products are shipped factory assembled and supplied with a no-hassle two-year warranty on parts and labor UNLESS specified otherwise.

1.1. What you need to complete the system:

PC-AT keyboard
(optional) 5.25" and/or 8" Floppy disk drive(s)
necessary peripheral cables
optional user-supplied PC ATX-style motherboard for internal mounting

If the user chooses to mount an ATX motherboard inside the IMSAI Series Two enclosure, a "download" cable may be connected between the IMSAI II parallel port and the corresponding ATX motherboard port. We will provide CP/M operating system support including a CBIOS driver on the IMSAI Series Two side that accesses the parallel port as if it were a disk drive. The PC software support includes a small software "server" that uses the native DOS/Windows/Linux file system to store files. This way, it becomes very easy to transfer programs from the web and run them on the Imsai II. Likewise, it is equally easy to transfer files from native Imsai and CP/M compatible disks (i.e. to convert files from 8" or 5.25") and store them on your PC.

2. Hardware Specification

2.1. Chassis

The IMSAI Series Two enclosure is modeled after the original **IMSAI 8080**, utilizing the same aluminum construction, familiar switch-and-LED layout, color, and finish as its predecessor. Most metal parts and the front panel are interchangeable with original **IMSAI 8080** enclosures, ensuring an upward path of enhancement for owners of older **IMSAI**'s. In addition, provision is made for installing two half-height 3.5" or 5" IDE devices inside the enclosure, in front of the power supply.

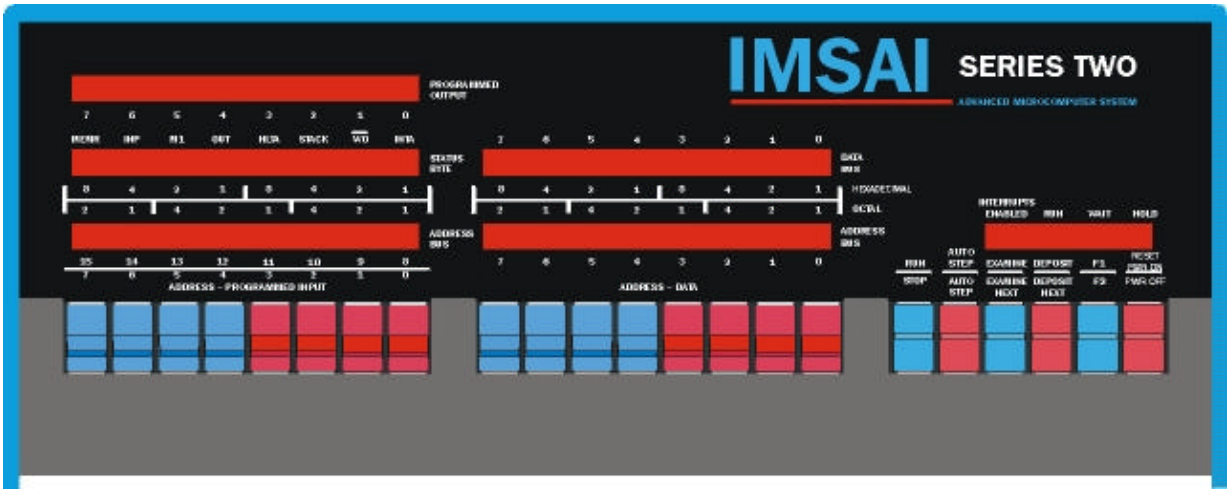


Figure 1: IMSAI Series Two – Front Panel

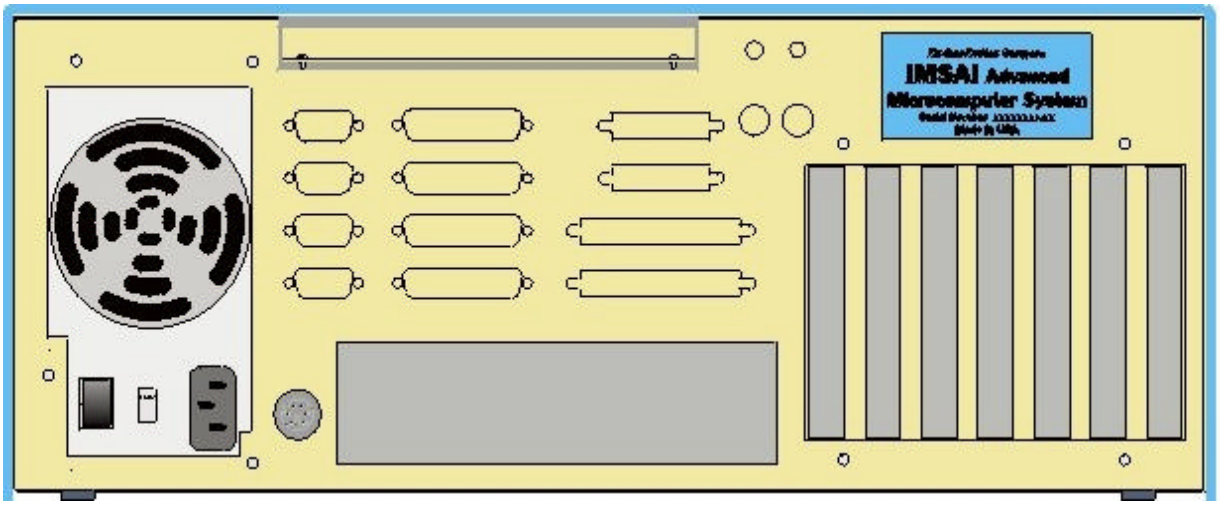


Figure 2: IMSAI Series Two – Rear Panel

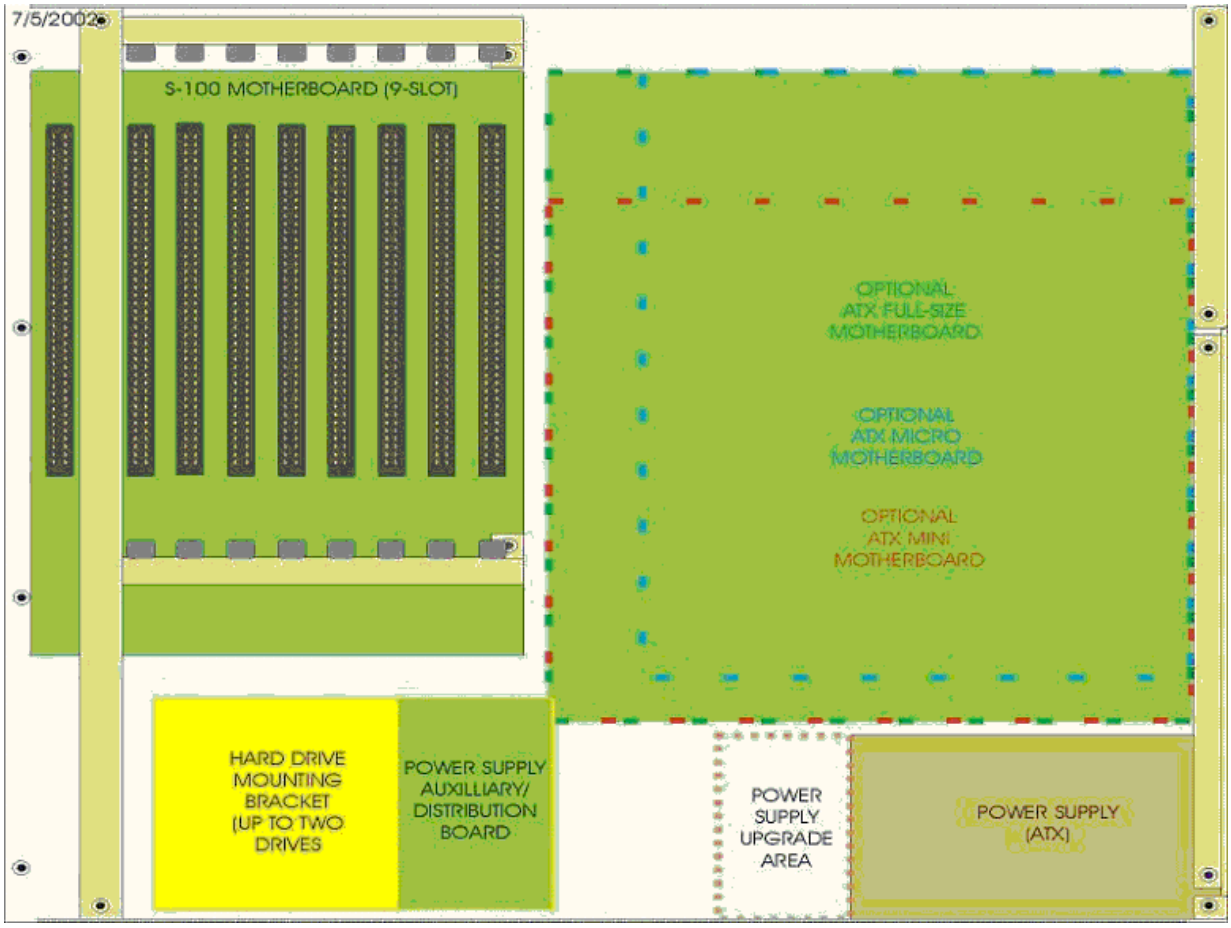


Figure 3: Internal Chassis Layout

2.2. Power Supply

System power is provided by a high quality PC ATX-style (2.03 spec.) switching supply that produces a safe UL/CSA-approved source of power superior in design to the original **IMSAI** PS-28 power supply. It also provides a convenient source of power for conventional floppy and hard disk drives, as well as CD ROM drives as used in today's PC architecture. Additionally, the power supply supports the remote power ON/OFF feature of the PC/ATX specification, and this feature is extended to the front panel. The supply can also provide power to an optional internal ATX motherboard. Input voltage is selectable by a slide switch for (typical) 90V~135VAC @ 13 amps, or 180V~265V AC @ 8 amps (47~63 Hz.). These specifications are subject to change without notice, and should be verified at time of order:

DC Output Load		Rated	Max	Min	Notes
+3.3V	(Amps)	14A	32A	0.3A	Max continuous total DC output power shall not exceed 350W.
+5V	(Amps)	20A	32A	0.3A	
+12V	(Amps)	8A	26A	1.5A	
-5V	(Amps)	.5A	1A	0A	Max combined output on 5V and +3.3V shall not exceed 185W.
-12V	(Amps)	.5A	1A	0A	
+5VSB	(Amps)	1A	2.2A	0.1A	

Figure 5: Standard 350W ATX Power Supply Output Currents

DC Output Load		Rated	Max	Min	Notes
+3.3V	(Amps)	40A	35A	0.3A	Max continuous total DC output power shall not exceed 460W.
+5V	(Amps)	46A	35A	0.3A	
+12V	(Amps)	24A	33A	1.5A	
-5V	(Amps)	1A	1A	0A	Max combined output on 5V and +3.3V shall not exceed 300W.
-12V	(Amps)	1A	1A	0A	
+5VSB	(Amps)	1.8A	2.2A	0.1A	

Figure 6: Optional 550W ATX Power Supply Output Currents

The 550W power supply is recommended for Pentium 4 and over-clocked ATX system motherboards.

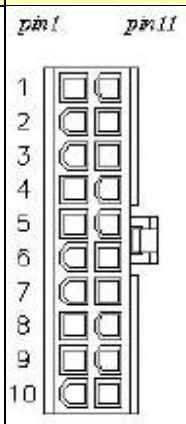
Signal	Color	Pin	Signal	Color	Pin	ATX Main Power Connector
+3.3VDC	Orange	1	+3.3VDC	Orange	11	
			+3.3V Sense	Brown		
+3.3VDC	Orange	2	-12VDC	Blue	12	
Common	Black	3	Common	Black	13	
+5VDC	Red	4	PS-ON	Green	14	
Common	Black	5	Common	Black	15	
+5VDC	Red	6	Common	Black	16	
Common	Black	7	Common	Black	17	
Common Sense	Black					
POK	Gray	8	-5VDC	White	18	
+5VSB	Purple	9	+5VDC	Red	19	
+12VDC	Yellow	10	+5VDC	Red	20	

Figure 7: ATX Main Power Connector

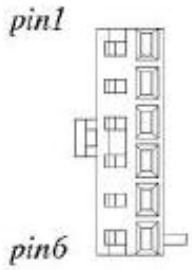
Signal	Color	Pin		Auxiliary Power Connector
Common	Black	1		
Common	Black	2		
Common	Black	3		
+3.3VDC	Orange	4		
+3.3VDC	Orange	5		
+5VDC	Red	6		

Figure 8: ATX Auxiliary Power Connector

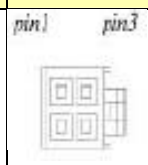
Signal	Color	Pin		+12V Power Connector
Common	Black	1		
Common	Black	2		
+12VDC	Yellow	3		
+12VDC	Yellow	4		

Figure 9: ATX 12V Power Connector

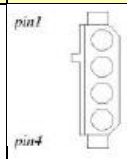
Signal	Color	Pin		Peripheral Connectors
+12VDC	Yellow	1		
Common	Black	2		
Common	Black	3		
+5VDC	Red	4		

Figure 10: Peripheral Connector

Signal	Color	Pin		3.5” Floppy Drive Connectors
+5VDC	Red	1		
Common	Black	2		
Common	Black	3		
+12VDC	Yellow	4		

Figure 11: Floppy Drive Connector

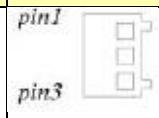
Signal	Color	Pin		Fan Connectors
Common	Black	1		
Fan Voltage	Red	2		
Fan Monitor	Yellow	3		

Figure 12: Fan Connector

2.3. Power Supply Booster

The IMSAI Series Two includes an auxiliary power supply board that plugs into the ATX power supply main connector. A small cable runs from the CPA Front Panel board for controlling the remote on/off function of the ATX power supply. The auxiliary power supply board also provides a power supply cable that plugs into an optional ATX internal motherboard. The +5 volt and +/- 12 volt supplies are tapped by boost circuitry to provide the necessary +8 and +/- 15 volts necessary for the S-100 bus.

The IEEE-696 S-100 specification for power distribution is:

+8 volts	Instantaneous minimum must be greater than +7 volts, instantaneous maximum less than 25 volts, and average maximum less than 11 volts.
+16 volts	Instantaneous minimum must be greater than 14.5 volts, instantaneous maximum less than 35 volts, and average maximum less than 21.5 volts.
-16 volts	Instantaneous maximum must be less than -14.5 volts, instantaneous minimum greater than -35 volts, and average minimum greater than -21.5 volts.

The power supply booster provides S-100 voltages toward the minimum side of the specifications to achieve better efficiency and to reduce thermal buildup, while ensuring good noise immunity through the S-100 board regulators. The tentative Series Two S-100 supply is:

+7.5 volts @ 14 amps
+15 volts @ 2 amps
-15 volts @ 0.5 amps

2.4. EXP-9/AT Backplane (Motherboard)

The IMSAI Series Two utilizes the IMSAI EXP-9/AT backplane designed with active termination and interleaved ground planes between lines, thus allowing S-100 boards to operate at 10 MHz. or higher. The IMSAI Series Two comes with a nine-slot active termination S-100 backplane standard (first slot reserved for the front panel.) A 20-slot EXP-20/AT backplane is optional. Please note that using the 20-slot backplane precludes mounting an ATX motherboard inside the enclosure.

The backplane is constructed of a sturdy 0.093" thick FR-4 laminate printed-circuit board and utilizes press-fit S-100 connectors. Power is supplied to the backplane via seven ¼" spade terminals. The backplane includes a header for connecting an external system reset switch if desired. Two test points are provided toward the front of the backplane to aid in measuring and adjusting the termination voltage.

Motherboard Reference	Description
JP1	External reset switch connector. The switch must have normally-open contacts and momentarily ground this signal to cause a system reset.
JP2	-16V Unregulated Power Supply Input
JP3	Ground
JP4	+16V Unregulated Power Supply Input
JP5	Ground
JP6	Ground
JP7	+8V Unregulated Power Supply Input
JP8	+8V Unregulated Power Supply Input
TP1	Ground
TP2	Termination Voltage
JH1-8	General-purpose IEEE-696 card slots.
JP9	Front panel card slot. (Electrically equivalent to JH1-8)
R11	Termination voltage adjustment. (Adjust to +2.7VDC)
D1	+8V Indicator LED
D2	+16V Indicator LED
D3	-16V Indicator LED

Figure 13: Backplane Connectors, Testpoints, and Calibration Points

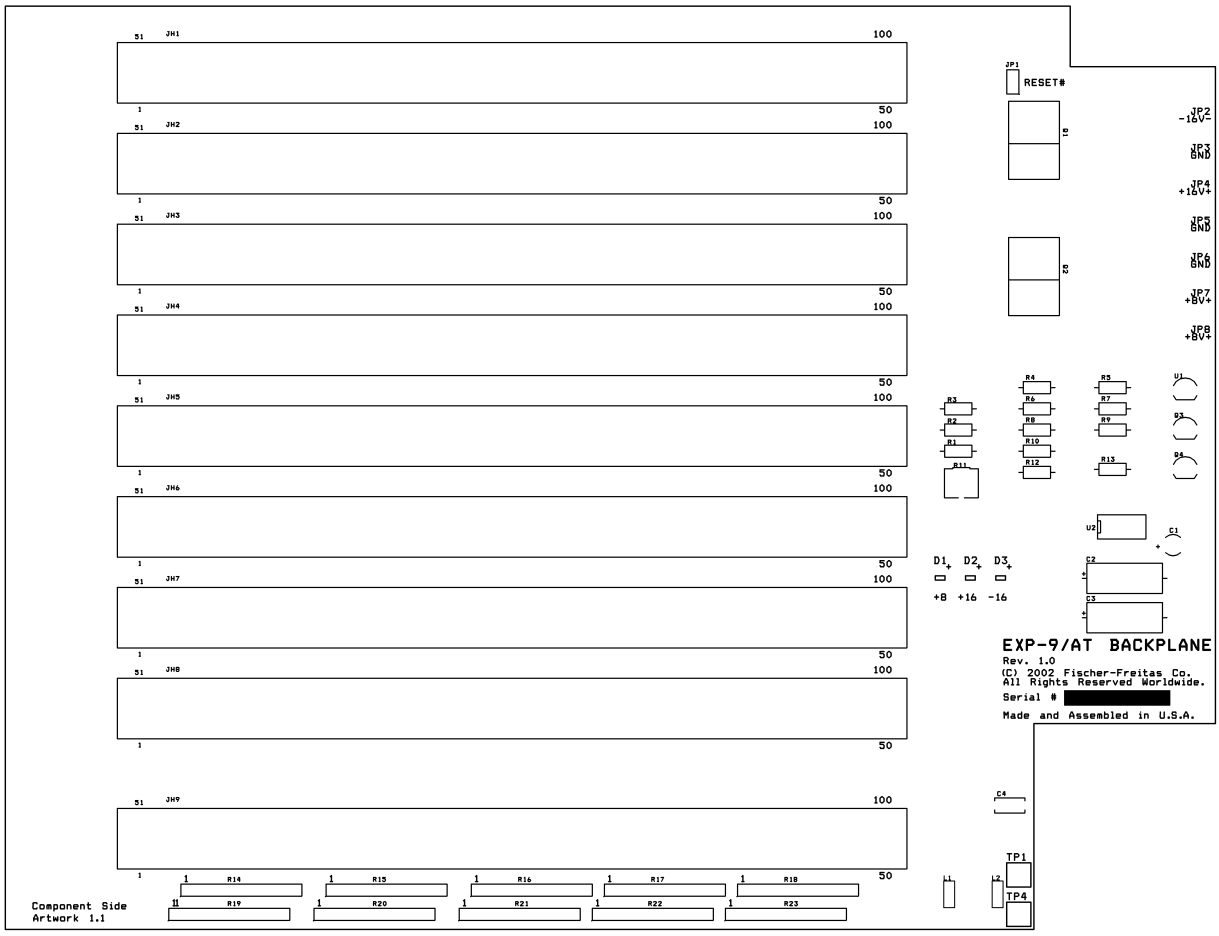
The termination voltage should be measured using an accurate voltmeter, and adjusted via R11 to 2.7V. Termination voltage can be measured by connecting voltmeter probes between TP1 and TP2.

NOTE:

DO NOT remove circuit boards from, or insert circuit boards into the backplane until voltage indicators D1, D2, and D3 are OFF. Damage to the backplane, connectors, and/or circuit boards may result if this precaution is not followed.

WARNING:

The mounting tab on transistor Q2 is live at the unregulated 8V input voltage potential. This transistor must be mounted securely to the backplane using an insulated Nylon screw. Care must be taken not to accidentally short this mounting tab to other parts of the backplane or chassis while power is applied to the system, or before voltage levels have bled down as indicated by D1, D2, and D3. Test this mounting tab before touching!



IEEE-696/S-100 Bus Signal Descriptions

Pin	Signal			Type	Description
1	+8V	B			Instantaneous minimum greater than 7 volts, instantaneous maximum less than 25 volts, average maximum less than 11 volts.
2	+16V	B			instantaneous minimum greater than 14.5 volts, instantaneous maximum less than 35 volts, average maximum less than 21.5 volts.
3	XRDY	S	H		One of two ready inputs to the current bus master. The bus is ready when both these ready inputs are true. See pin 72.
4	VI0*	S	L	O.C.	Vectored interrupt line 0
5	VI1*	S	L	O.C.	Vectored interrupt line 1
6	VI2*	S	L	O.C.	Vectored interrupt line 2
7	VI3*	S	L	O.C.	Vectored interrupt line 3
8	VI4*	S	L	O.C.	Vectored interrupt line 4
9	VI5*	S	L	O.C.	Vectored interrupt line 5
10	VI6*	S	L	O.C.	Vectored interrupt line 6
11	VI7*	S	L	O.C.	Vectored interrupt line 7
12	NMI*	S	L	O.C.	Non-maskable interrupt.
13	PWRFAIL*	B	L		Power fail bus signal. (See Section 2.10.1 regarding pseudo open collector nature)
14	DMA3*	M	L	O.C.	Temporary master priority bit 3.
15	A18	M	H		Extended address bit 18.
16	A17	M	H		Extended address bit 17.
17	A16	M	H		Extended address bit 16.
18	SDSB*	M	L	O.C.	The control signal to disable the 8 status signals.
19	CDSB*	M	L	O.C.	The control signal to disable the 5 control output signals.
20	GND	B			Common with pin 100.
21	NDEF				Not to be defined. Manufacturer must specify any use in detail.
22	ADSB*	M	L.	O.C.	The control signal to disable the 16 address signals.
23	DODSB*	M	L	O.C.	The control signal to disable the 8 data output signals.
24	Phi?	B	H		The master timing signal for the bus.
25	pSTVAL*	M	L		Status valid strobe.
26	pHLDA	M	H		A control signal used in conjunction with HOLD* to coordinate bus master transfer operations.
27	RFU				Reserved for future use.
28	RFU				Reserved for future use.
29	A5	M	H		Address bit 5.

30	A4	M	H		Address bit 4.
31	A3	M	H		Address bit 3.
32	A15	M	H		Address bit 15 (most significant for non-extended addressing.)
33	A12	M	H		Address bit 12.
34	A9	M	H		Address bit 9.
35	D01 [DATA1]	M [M/S]	H		Data out bit 1, bi-directional data bit 1.
36	DO0 [DATA0]	M [M/S]	H		Data out bit 0, bi-directional data bit 0.
37	A10	M	H		Address bit 10.
38	D04 [DATA4]	M [M/S]	H		Data out bit 4, bi-directional data bit 4.
39	D05 [DATA5]	M [M/S]	H		Data out bit 5, bi-directional data bit 5.
40	DO6 [DATA6]	M [M/S]	H		Data out bit 6, bi-directional data bit 6.
41	DI2 [DATA10]	S [M/S]	H		Data in bit 2, bi-directional data bit 10.
42	DI3 [DATA11]	S [M/S]	H		Data in bit 3, bi-directional data bit 11.
43	DI7 [DATA15]	S [M/S]	H		Data in bit 7, bi-directional data bit 15.
44	SM1	M	H		The status signal which indicates that the current cycle is an op-code fetch.
45	sOUT	M	H		The status signal identifying the data transfer bus cycle to an output device.
46	sINP	M	H		The status signal identifying the data transfer bus cycle from an input device.
47	sMEMR	M	H		The status signal identifying bus cycles which transfer data from memory to a bus master, which are not interrupt acknowledge instruction fetch cycle(s).

48	SHLTA	M	H		The status signal which acknowledges that a HILT instruction has been executed.
49	CLOCK	B			2 MHz (0.5°/) 40-60% duty cycle. Not required to be synchronous with any other bus signal.
50	GND	B			Common with pin 100.
51	+8 VOLTS	B			Common with pin 1.
52	-16 VOLTS	B			Instantaneous maximum less than -14.5 volts, instantaneous minimum greater than -35 volts, average minimum greater than -21.5 volts.
53	GND	B			Common with pin 100.
54	SLAVE CLR*	B	L	O.C.	A reset signal to reset bus slaves. Must be active with POC* and may also be generated by external means.
55	DMA0*	M	L	O.C.	Temporary master priority bit 0.
56	DMA1*	M	L	O.C.	Temporary master priority bit 1.
57	DMA2*	M	L	O.C.	Temporary master priority bit 2.
58	sXTRQ*	M	L		The status signal which requests 16-bit slaves to assert SIXTN*.
59	A19	M	H		Extended address bit 19.
60	SIXTN*	S	L	O.C.	The signal generated by 16-bit slaves in response to the 16-bit request signal sXTRQ*
61	A20	M	H		Extended address bit 20.
62	A21	M	H		Extended address bit 21.
63	A22	M	H		Extended address bit 22.
64	A23	M	H		Extended address bit 23.
65	NDEF				Not to be defined signal.
66	NDEF				Not to be defined signal.
67	PHANTOM*	M/S	L	O.C.	A bus signal which disables normal slave devices and enables phantom slaves-primarily used for bootstrapping systems without hardware front panels.
68	MWRT	B	H		pWR•-sOUT (logic equation). This signal must follow pWR* by not more than 30 ns. (See note, Section 2.7.5.3)
69	RFU				Reserved for future use.
70	GND	B			Common with pin 100.
71	RFU				Reserved for future use.
72	RDY	S	H	O.C.	See comments for pin 3.

73	INT*	S	L	O.C.	The primary interrupt request bus signal.
74	HOLD*	M	L	O.C.	The control signal used in conjunction with pHLDA to coordinate bus master transfer operations.
75	RESET*	B	L	O.C.	The reset signal to reset bus master devices. This signal must be active with POC* and may also be generated by external means.
76	pSYNC	M	H		The control signal identifying BS1.
77	pWR*	M	L		The control signal signifying the presence of valid data on DO bus or data bus.
78	pDBIN	M	H		The control signal that requests data on the DI bus or data bus from the currently addressed slave.
79	AO	M	H		Address bit 0 (least significant).
80	A1	M	H		Address bit 1.
81	A2	M	H		Address bit 2.
82	A6	M	H		Address bit 6.
83	A7	M	H		Address bit 7.
84	A8	M	H		Address bit 8.
85	A13	M	H		Address bit 13.
86	A14	M	H		Address bit 14.
87	A11	M	H		Address bit 11.
88	D02 [DATA2]	M [M/S]	H		Data out bit 2, bi-directional data bit 2.
89	D03 [DATA3]	M [M/S]	H		Data out bit 3, bi-directional data bit 3.
90	D07 [DATA7]	M [M/S]	H		Data out bit 7, bi-directional data bit 7.
91	DI4 [DATA12]	S [M/S]	H		Data in bit 4 and bi-directional data bit 12.
92	DI5 [DATA13	S [M/	H		Data in bit 5 and bi-directional data bit 13.

	]	S]			
93	DI6 [DATA14]	S [M/ S]	H		Data in bit 6 and bi-directional data bit 14.
94	DI1 [DATA9]	S [M/ S]	H		Data in bit 1 and bi-directional data bit 9.
95	DI0 [DATA8]	S [M/ S]	H		Data in bit 0 (least significant for 8-bit data) and bi-directional data bit 8.
96	sINTA	M	H		The status signal identifying the bus input cycle(s) that may follow an accepted interrupt request presented on INT*.
97	sW0*	M	L		The status signal identifying a bus cycle which transfers data from a bus master to a slave.
98	ERROR*	S	L	O.C .	The bus status signal signifying an error condition during present bus cycle.
99	POC*	B	L		The power-on clear signal for all bus devices; when this signal goes low, it must stay low for at least 10 milliseconds.
10 0	GND	B			System ground.

B – Bus signal from Power Supply or CPA.
S – Slave generated signal.
M – Master Generated signal
M/S – Master or Slave Generated signal.
* - Signal is TRUE when active low
H – Active High
L – Active Low

2.5. MPU-C Processor Board

The IMSAI Series Two utilizes the Zilog Z8S180 microprocessor and provides a complete system on an IEEE-696 compatible S-100 board. The MPU-C consists of the following on-board subsystems:

Microprocessor – Zilog Z8S180 CPU
Memory Subsystem (SRAM, FLASH, EPROM)
I/O Subsystem
IEEE-696 and to Z8S180 Localbus Bridge
Priority Interrupt Controller Subsystem
Temporary Master Access (TMA) Subsystem
Voltage Regulator Subsystem
In-Circuit-Programming interface for programmable logic components.

Zilog Z8S180 Microprocessor

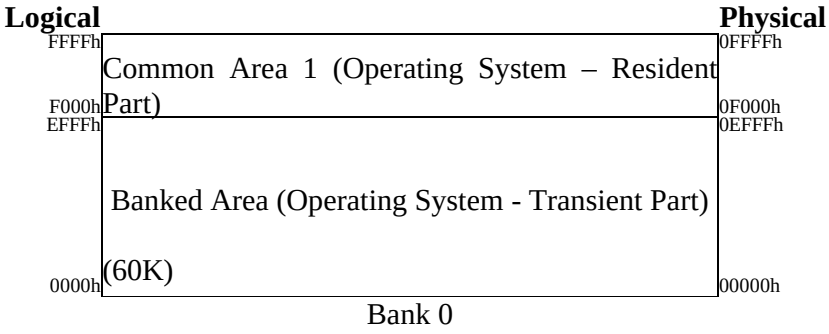
The Z8S180 microprocessor is based on a microcoded execution unit and advanced CMOS manufacturing technology. It is an 8-bit CPU that offers high-performance while retaining software compatibility with the Zilog Z80 CPU. In addition, the Z8S180 offers on-chip peripherals including:

- Dual-channel DMA controller
- Memory Management Unit (MMU)
- Wait State Generator
- Two UARTS
- Two 16-bit Timer Channels
- Interrupt Controller

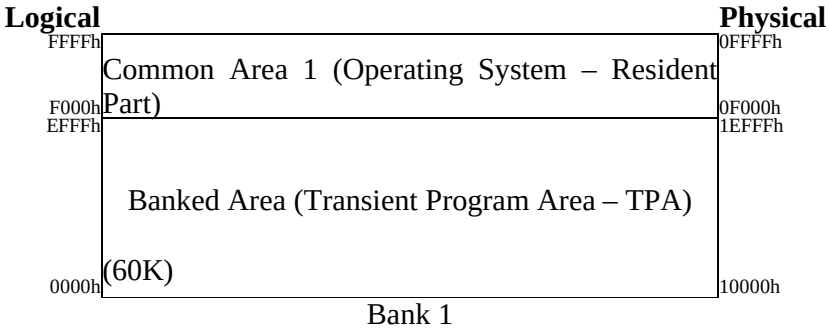
The Z8S180 is code compatible with the Z80 CPU, and offers increased performance by virtue of higher operating frequencies, reduced instruction execution times, an enhanced instruction set, and an on-chip memory management unit (MMU) with the capability of addressing up to 1MB of memory.

The MMU allows pages of memory to be mapped into the Z8S180's 64KB logical address space. The 64KB logical address space is interpreted by the MMU as consisting of up to three separate logical address areas: Common Area 0, Bank Area, and Common Area 1. The boundaries between Common and Bank Areas can be programmed with a 4KB resolution.

Upon reset, memory is organized as a single common area from physical address 0000h-FFFFh. The CP/M CBIOS initialization routine partitions the memory as a 60KB banked area, and a 4KB Common Area 1. Common Area 0 is not used.



Bank 0



Bank 1

Memory Subsystem

The MPU-C board contains 1MB of static RAM (SRAM), one 128K FLASH EPROM, and provision for one JEDEC compatible 8, 16, or 32KB PROM/EPROM. The FLASH EPROM overlays SRAM from physical address 00000h-1FFFFh. This allows the Z8S180 to start execution from FLASH upon system reset. The FLASH may be relocated to physical address 80000h-9FFFFh, and may also be disabled completely. FLASH relocation can be used when portions of the FLASH contain CBIOS or operating system code, or when reprogramming the FLASH. The PROM/EPROM resides in page 15 and may be relocated to Page 7. The precise location of the PROM device depends on the ROM_SIZE[1:0] bits of the MPU-C Memory Control Register (MCR) as described in Figure15.

In addition to the Z8S180's on-chip MMU, the MPU-C contains additional memory management hardware to provide maximum flexibility to the user. This memory management hardware provides two memory models: *large* and *small*.

The default memory model is the *small memory model*. When the *small memory model* is selected, a portion of each type of MPU-C on-board memory resource is available in 64K of address space. The *small memory model* is useful when programming from the CPA, and when using an operating system that does not take advantage of the Z8S180's 1Mb address range.

The following diagram illustrates the physical memory map of the MPU-C on-board memory resources. Each of the 16 pages is 64KB in size for a total of 1MB of addressable memory. Shaded regions illustrate default placement of FLASH and EPROM resources. The leftmost column shows the physical addresses of memory resources in the *large memory model* while the rightmost column shows the physical addresses of memory resources in the *small memory model.*

When the large memory model is selected, all of the MPU-C memory resources are available for selection by the Z8S180's MMU.

When *small memory model* is selected, a 4KB portion of physical memory is carved from each 64KB page and placed into Page 0. In *small memory model* there is no need to use the Z8S180's MMU. *Small memory model* is implemented in hardware by steering CPU Address bits [15:12] to the memory subsystem's Address bits [19:16]. During *small memory model* operation, the memory subsystem's address bits [15:12] are always zero. The 4K blocks to the right of the squiggily line in *figure 13* depict the portion of physical memory addressable in the *small memory model.*

Writes to FLASH or EPROM areas cause writes to the SRAM at the same memory locations. Reads from FLASH or EPROM come from the FLASH or EPROM device. This feature allows bootstrap code to be copied in-place to SRAM, allowing bootstrap code to copy itself, swap out the FLASH, and then continue executing from SRAM.

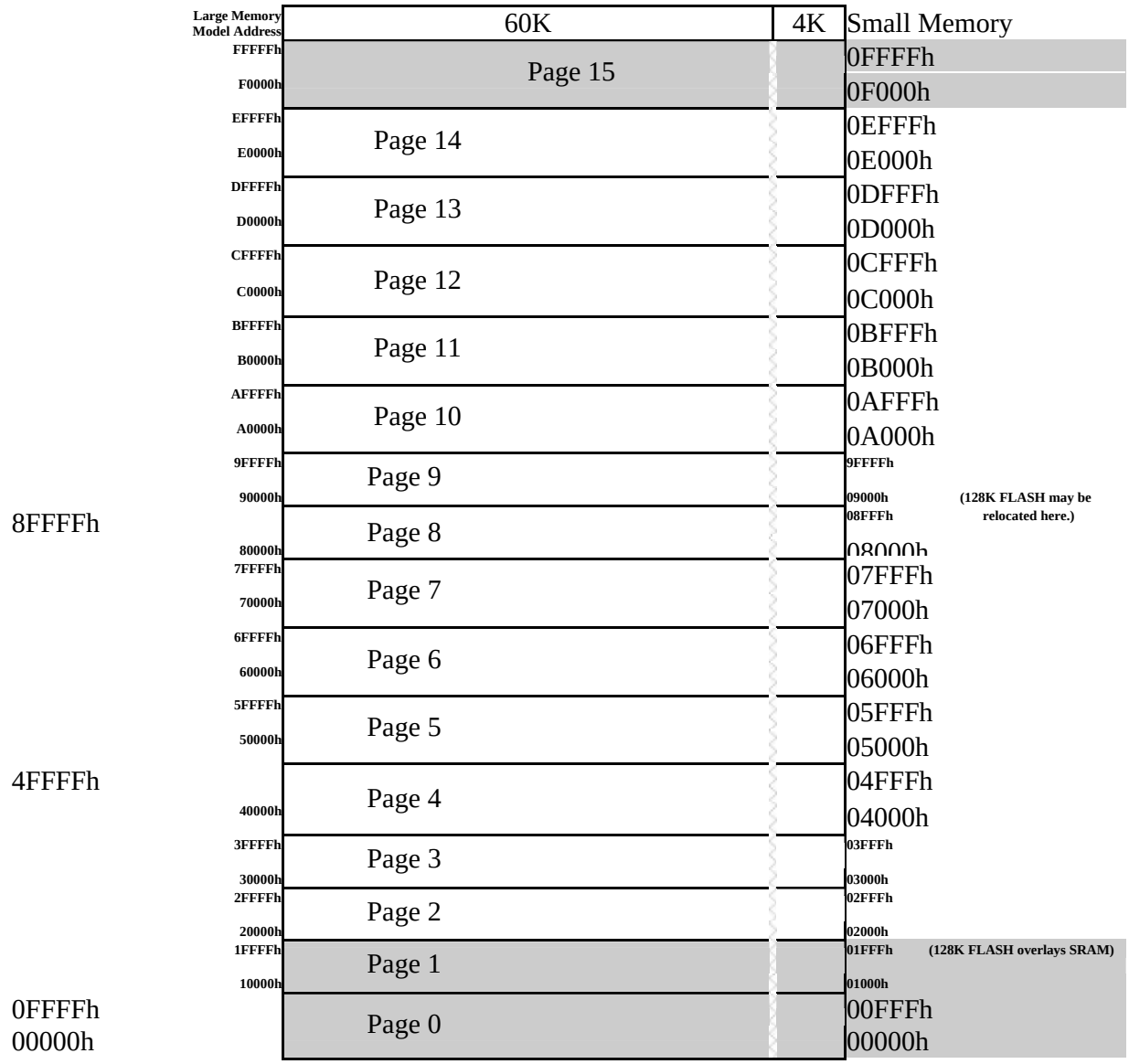


Figure 14: Physical Memory Map

A jumper on the MPU-C board (W?) allows swapping the FLASH and EPROM locations so that the system can be booted from FLASH or EPROM. This feature also allows a "failsafe" bootstrap to be loaded in EPROM so that in case the FLASH bootstrap becomes corrupt, the MPU-C can be booted from EPROM.

MPU-C Memory control register:

	7	6	5	4	3	2	1	0
Mnemonic	MMODEL	FL_RELOC	FL_PGM_EN	FLASH_DIS		ROM_RELOC	ROM_SIZE1	ROM
Reset	0	0	0	0	0	0	0	0
R/W	W	W	W	W		W	W	W

Figure 15: Memory Control Register

Bit Definitions:

MMODEL: This bit selects between "small" and "large" memory models. Setting this bit selects the large memory model, while clearing it selects the small memory model.

FL_RELOC: This bit relocates the FLASH memory from pages 0 and 1 to pages 8 and 9 when set.

FL_PGM_EN This bit enables writes to the FLASH EPROM when set. When cleared, writes propagate to the underlying SRAM.

FLASH_DIS This bit enables reads from the FLASH EPROM. Writes always propagate to the underlying SRAM unless the FL_PGM_EN bit is set.

ROM_RELOC: This bit relocates the ROM memory from page 15 to page 7 when set.

ROM_SIZE[1:0]: These bits select the size of the ROM as illustrated in the following table:

ROM_SIZE1	ROM_SIZE0	ROM Size (Kb)	Address Range
0	0	ROM Disabled	----------
0	1	8Kb (2764)	FE000h-FFFFFh
1	0	16Kb (27128)	FC000h-FFFFFh
1	1	32Kb (27256)	F8000h-FFFFFh

Figure 16: ROM Size Selection Bit Definition

I/O Subsystem

The Z8S180, like the Z80, provides 64K of I/O address space. Address bits A[15:8] contain the current value of the A register. Address bits A[7:0] are supplied in the I/O instruction itself. In order to maintain code compatibility with earlier S-100 systems which utilized only 256 bytes of I/O space, only 8-bits of I/O address need be decoded by adapters on the S-100 bus. I/O devices on the MPU-C board or on the S-100 bus may decode more bits of I/O address space as long as they also claim all "shadows" of this space. The MPU-C does *not* support address mirroring (duplicating A[7:0] on A[15:8]).

For example:

An adapter requiring 16 bytes of I/O space may use: 080h-084h, 180-184h, 280h-284h, 380h-384h...

... as long as no other adapter on the S-100 bus uses the address 080h-084h. This allows complex adapters to consume large amounts of I/O space without having to use up valuable space in the 0000h-00FFh region. In the example above, the adapter would need to decode at least 10-bits of I/O address (A[9:0]). It is strongly suggested that new S-100 adapters decode at least 12-bits of address even if all of the addresses used by the adapter require less decoding. This practice facilitates better use of the Z8S180's 64K I/O space.

The Z8S180 contains 64-bytes of internal I/O registers. These registers default to I/O addresses 0000h-003Fh on reset, but may be relocated to any 64-byte boundary in the range of 0000h-00FFh. This means that these registers may reside at 0000h-003Fh, 0040h-007Fh, 0080-00BFh, or 00C0-00FFh. The internal registers fully decode the 16-bit I/O address space.

The MPU-C and Multi-I/O boards contain various registers addressed via I/O ports. These registers are programmed to the I/O locations shown below via the bootstrap firmware. All registers may, with the exception of the keyboard controller and the real-time clock, be relocated in the range of 0000h-03FFh via software. This allows the MPU-C registers to be relocated in case of conflict with existing S-100 adapters. All on-board registers fully decode the 16-bit I/O address space.

I/O Port	Description
0000h-003Fh	Z8S180 Internal I/O Registers
0070h-0077h	CPA Front Panel
0078h-007Fh	MPU-C on-board registers
0080h-00FFh	Super I/O Controller

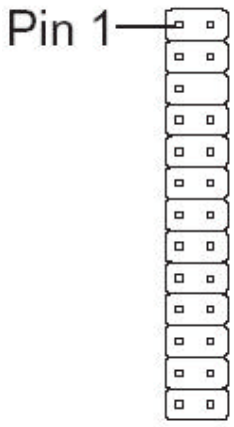
Figure 17: IMSAI Series Two I/O Map

MPU-C IEEE-696 Bus Interface and Localbus Bridge

The MPU-C provides various jumpers (W*) on-board which allow the selection of various S-100 bus pin definitions to maintain compatibility with the original Altair/IMSAI S-100 bus, or with the IEEE-696 S-100 bus standard. The MPU-C is shipped with jumper settings configured for IEEE-696 compatibility. The user may reconfigure one or more of these signals for the Altair/IMSAI bus for compatibility with non-IEEE-696 compliant S-100 cards. Please note that the CPA-5 and MPU-C boards use a 26-pin ribbon cable for connectivity between the CPA and MPU-C. In addition to the CPA bi-directional data bus, this cable carries the CPA signals RUN, SS, SSWDSB#, and XRDY. This allows IEEE-696 compatibility to be achieved in front-panel systems such as the Series Two. If you require these signals on the S-100 bus, then jumpers on the CPA and MPU-C should be set accordingly, and pins 17-26 on the CPA/MPU-C ribbon cable must be disconnected.

The MPU-C jumpers and testpoints are described below:

Jumper W1	Description (When jumper is inserted)	Notes	
1-2	XRDY on S-100 bus pin 3	A/I	
3-4	SSWDSB# on S-100 bus pin 53	A/I	
3-5	S-100 bus pin 53 is GND	IEEE-696 [DEFAULT]	
5-6	Invalid jumper setting.	Do not jumper	
7-8	NDEF on S-100 bus pin 65 is connected to Z8S180 DREQ0#	Series Two Specific setting [DEFAULT]	
9-10	NDEF on S-100 bus pin 66 is connected to Z8S180 REFRESH# output	Non A/I, Non IEEE-696, used by some dynamic RAM boards.	
11-12	RFU on S-100 bus pin 69 is connected to Z8S180 TEND0#	Series Two Specific setting [DEFAULT]	
13-14	S-100 bus pin 20 is connected to GND	IEEE-696 [DEFAULT]	
15-16	S-100 bus pin 70 is connected to GND	IEEE-696 [DEFAULT]	
17-18	SS on pin 21	A/I	
19-20	RUN on S-100 bus pin 71	A/I	
21-22	RFU on S-100 bus pin 27 is connected to Z8S180 DREQ1#	Series Two Specific setting [DEFAULT]	
23-24	RFU on S-100 bus pin 28 is connected to Z8S180 TEND1#	Series Two Specific setting [DEFAULT]	
25-26	Slave Mode Enable	For debug only.	
Note: odd pins on Jumper block W1 may be used as testpoints to their respective S-100 bus signals. Odd pins are connected to the S-100 bus, while even pins are connected to the MPU-C local bus.			



Additional MPU-C Testpoints:

S-100 Signal	Description	S-100 Bus Pin	Testpoint
VSS_-16V	A/I Bus, IEEE-696 bus –16V unregulated supply	52	8
SIXTN#	IEEE-696 Bus SIXTN# signal	60	5
SXTRQ#	IEEE-696 Bus sXTRQ# signal	58	4
VCC_16V	A/I Bus, IEEE-696 Bus +16V unregulated supply	2	3

Figure 18: MPU-C Test Points

Hardware Interrupts

The Z8S180 processor has 12 internal levels of interrupts. Four of these interrupts are generated from external sources: NMI, INT0, INT1, and INT2. The remaining eight interrupts are sourced within the peripheral blocks of the Z8S180 itself.

The MPU-C employs an 8259A-compatible priority interrupt controllers (PICs) to handle external interrupts. The PIC interrupts the Z8S180 on the INT0 input. The Z8S180 INT0 input is configured for Mode 0 which causes an instruction fetch from the data bus upon acknowledgement of an interrupt. Mode 0 is the mode which maintains the "software compatibility" with the 8080. In this mode, during the interrupt acknowledge (INTACK) cycle, the Z8S180 fetches the data on the bus as an "instruction" and executes it, like the 8080. From a hardware standpoint, compatibility with the 8080 is not maintained: the 8080 generates three INTA pulses during the interrupt acknowledge cycle, while the Z8S180 generates only one INTACK signal (which can be decoded from /M1 and /RD). This system works well with systems that put a "RST" (restart) instruction onto the bus during the Interrupt acknowledge cycle, which is a one-byte instruction. In order to use an 8259A with the Z8S180, three INTA pulses must be generated during the INTACK cycle.

The following figure depicts the logic required to emulate the 8080 INTACK cycle. This circuit works as follows *(assume that the instruction sent by the 8259 was a "CALL" instruction)*. On interrupt acknowledge cycle, a decoded INTA signal is sent out as an INTA pulse for the 8259 and at the same time, sets the flip-flop to indicate that the interrupt acknowledge cycle is started. On the following memory read cycle of the jump address for the call instruction, this circuit generates two additional INTA pulses for the 8259A and also masks off the read signal for the memory to avoid bus contention problems. On the following write cycle, /WR signal resets the flip-flop to indicate that the interrupt acknowledge cycle is completed.

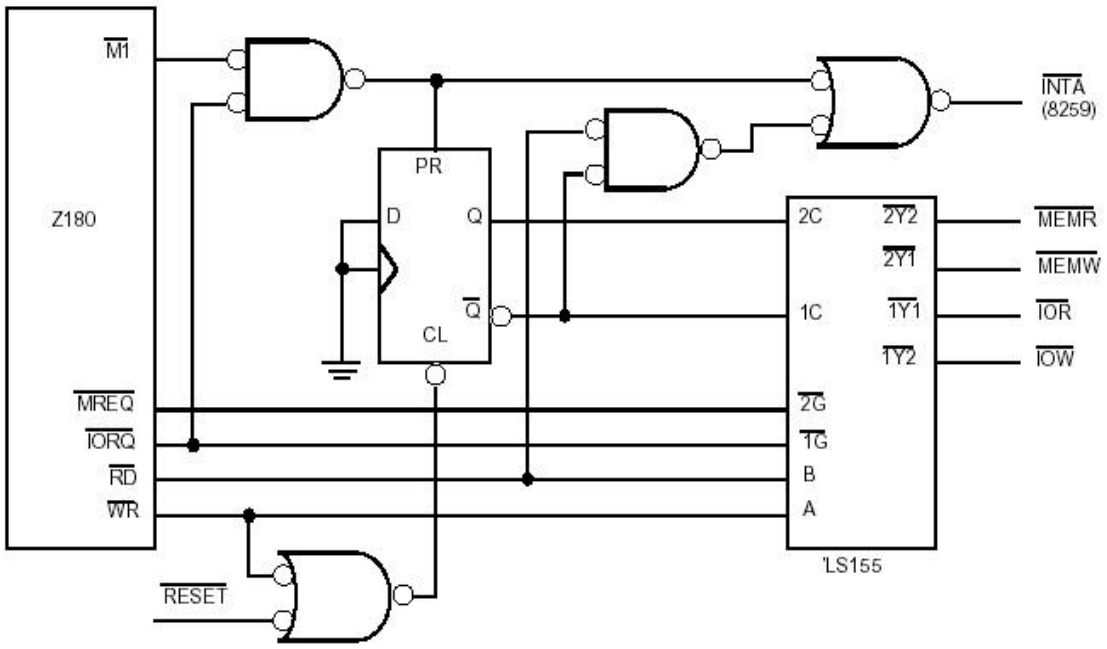


Figure 19: Interfacing the 8259A to the Z8S180

Interrupts originating from the SMC Super I/O controller may be configured to occur on any of the S-100 bus as vectored interrupt lines (VI0-VI7.)

	CPU	8259A	Description
High Priority	1		TRAP (Undefined Opcode Trap)
	2		NMI (Non-maskable interrupt)
	3	0	S-100 VI0
		1	S-100 VI1
		2	S-100 VI2
		3	S-100 VI3
		4	S-100 VI4
		5	S-100 VI5
		6	S-100 VI6
		7	S-100 VI7
	4		Reserved (External Interrupt 1)
	5		Reserved (External Interrupt 2)
	6		Timer 0
	7		Timer 1
	8		DMA Channel 0
	9		DMA Channel 1
	10		Clocked Serial I/O Port
Low Priority	11		Serial Port 0 (MPU-C)
	12		Serial Port 1 (MPU-C)

Figure 20: MPU-C Interrupt Priorities

Direct Memory Access

The MPU-C supports Direct Memory Access (DMA) via the Z8S180's internal DMA controller. The MPU-C is capable of memory to memory DMA, as well as memory to I/O DMA. In addition, the MPU-C supports IEEE-696 Temporary Master Access (TMA) to support existing S-100 adapters that utilize TMA.

MPU-C SLAVE Mode

The MPU-C supports a SLAVE mode which is primarily a debugging and testing mode. In this mode, the IEEE-696 to Localbus Bridge is configured as an IEEE-696 Temporary Master, and the direction of certain MPU-C bus transceivers is reversed. Slave mode allows the MPU-C to be used in a multiprocessor configuration. This requires custom code in the IEEE-696 to Localbus Bridge chip. Fischer-Freitas Company does not support this code. Under normal circumstances, the SLAVE MODE jumper should never be selected, as this could cause electrical contention on the S-100 backplane and between S-100 cards, resulting in permanent damage to your system. SLAVE Mode is described here for the adventurous and to help document how the MPU-C supports IEEE-696 Temporary Master Access (TMA.)

MPU-C Connector Pinouts

Signal	Description	Direction	MPU-C 2x5 Header Pin Number	DB9-M Connector on Cabinet	DB25-M Connector on Cabinet	
DCD	Data Carrier Detect	In	1	1	8	
N/C	No Connect	-	2	6	6	
RxD	Receive Data	In	3	2	3	
RTS	Request to Send	Out	4	7	4	
TxD	Transmit Data	Out	5	3	2	
CTS	Clear to Send	In	6	8	5	
N/C	No Connect	Out	7	4	20	
N/C	No Connect	In	8	9	22	
GND	Signal Ground	-	9	5	7	
-	Key	-	10	-	-	

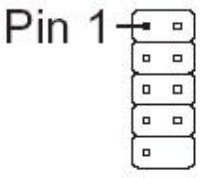


Figure 21: MPU-C Serial Port 0

Signal	Description	Direction	MPU-C 2x5 Header Pin Number	DB9-M Connector on Cabinet	DB25-M Connector on Cabinet	
N/C	No Connect	-	1	1	8	
N/C	No Connect	-	2	6	6	
RxD	Receive Data	In	3	2	3	
N/C	No Connect	-	4	7	4	
TxD	Transmit Data	Out	5	3	2	
CTS	Clear to Send	In	6	8	5	
N/C	No Connect	-	7	4	20	
N/C	No Connect	-	8	9	22	
GND	Signal Ground	-	9	5	7	
-	Key	-	10	-	-	

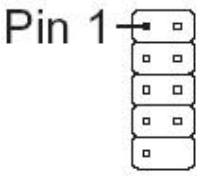


Figure 22: MPU-C Serial Port 1

Signal	Description	Direction	MPU-C 2x13eader Pin Number		
CPA_D0	Control Panel Data 0	I/O	2		
CPA_D1	Control Panel Data 1	I/O	4		
CPA_D2	Control Panel Data 2	I/O	6		
CPA_D3	Control Panel Data 3	I/O	8		
CPA_D4	Control Panel Data 4	I/O	10		
CPA_D5	Control Panel Data 5	I/O	12		
CPA_D6	Control Panel Data 6	I/O	14		
CPA_D7	Control Panel Data 7	I/O	16		
-	Key	-	18		
RUN	Control Panel RUN	In	20		
SS	Control Panel Single-step	In	22		
SSWDSB#	Control Panel Sense Switch Disable	In	24		
XRDY	Control Panel Ready	In	26		
GND	Signal Ground	-	Odd Pins		

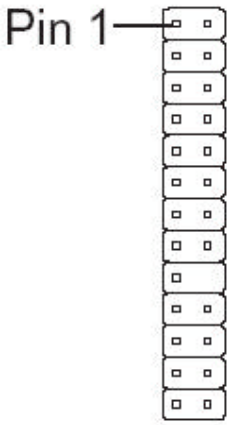


Figure 23: MPU-C CPA Connector

2.6. CPA Programmer's Front Panel

The IMSAI Series Two CPA Programmer's Front Panel provides the user with a means of monitoring and control of program and data by means of LED indicators and front panel switches. ADDRESS, DATA, STATUS and processor information indicated by respective LED indicators, each clearly labeled on the front panel mask.

The front panel switches allow direct examination and control of any selected memory location in the 64KB logical address space currently in use by the Z8S180 processor. The CPA is always in sync with the Z8S180's 64KB logical address space as determined by the Z8S180's internal MMU, and the MPU-C Memory Control Register (MCR). Neither the Z8S180's internal MMU nor the MPU-C MCR Register may be changed via the CPA. For this reason, the *small memory* model (see section 2.5.2) is provided for users who wish to access a combination of SRAM, FLASH, and EPROM simultaneously from the front panel.

Eight switches and 8 LEDs combine to offer a user-programmable input/output port for low-level programming or testing. The newly enhanced SINGLE/AUTO STEP switch allows the user to "single-step" or "auto-step" through program memory while monitoring data, address, and control word information on the LED's.

The "single-step" feature is activated by raising or lowering the SINGLE/AUTO STEP switch for each step. If held in either the up or down position, the "auto-step" feature will automatically step through the program at about one step every 1 1/2 seconds for eight counts, then increase to a user-adjustable rate of approximately 1 to 5 steps per second.

The CPA also incorporates an IEEE-696 compatible ERROR TRAP circuit, which allows the user to capture and recover the low and high INSTRUCTION FETCH address prior to an ERROR condition, set by the ERROR* line (pin 98 of the S-100 bus). The low and high bytes of the 64K address bus are latched into a pair of 8-bit latches on each FETCH instruction of the program, and these latches are mapped to two of four contiguous I/O addresses (base+1 and base+2). An I/O read to the base+0 address will clear the latches of the old address and allow loading of the current address upon the next FETCH instruction. The base+3 address is reserved for expansion options.

The user may set the base address to one of 64 I/O addresses by means of an on-board 8-position dip switch. The ERROR* line (pin 98 of the bus) is factory jumpered to the NMI* (Non Maskable Interrupt) pin of the bus, so that a user-defined error recovery routine may be implemented. This jumper may also be routed to any other vectored interrupt line, if desired.
The IMSAI Series Two CPA Programmer's Front Panel is fully compatible with Altair/IMSAI and IEEE-696 S-100 boards, and may be used in early IMSAI enclosures and systems with no modification required. Jumpers are provided to allow for conflicting bus definitions between early and late S-100 specifications. It will serve as an exact mechanical replacement for the original IMSAI 8080 CPA Programmer's Front Panel.

2.7. IMSAI Super-I/O Board

The IMSAI Super I./O Controller Board provides a complete I/O subsystem for the IEEE-696 bus. The Super I/O Controller supports 8-bit address decoding for compatibility with the original IMSAI 8080 and other S-100 bus systems as well as enhanced 16-bit address decoding supported by the MPU-C processor board in the IMSAI Series Two. The Super-I/O controller also supports DMA for floppy disk access via the MPU-C on-board DMA controller. The Super-I/O controller does not support IEEE-696 Temporary Master Access (TMA.)

The Super I/O Controller provides the following features:

- Standard Microsystems Corporation (SMC) FDC37C935APM Super I/O Controller.
- Support for two Floppy Diskette drives, in any combination:
- 3.5-inch 2.88MB, 1.44MB, 720KB.
- 5.25-inch 1.2MB, 360KB, DS/HD, DS/DD, SS/DD, SS/SD.
- 8-inch Single or Double-Density.
- Two NS16550-compatible UARTS.
- One IEEE-1284-compatible parallel port.
- PS/2-compatible keyboard/mouse controller.
- Two independent IDE channels supporting up to two IDE devices each.
- Battery backed real-time clock/calendar with non-volatile RAM.
- 128KB FLASH memory with banked memory support and selectable window size.

Device	I/O Range	FDC37C935APM Configured for Address:
IEEE-696 Bridge	80-83	N/A
Parallel Port	88-8F	0x308-30F
Floppy	90-97	0x310-317
Floppy (DMA)	98-9F	0x318-31F
Serial 0	A0-A7	0x320-327
Serial 1	A8-AF	0x328-32F
IDE0	B0-B7	0x330-337
IDE0	B8	0x338
IDE1	C0-C7	0x340-347
IDE1	C8	0x348
Keyboard/Mouse	E0,E4	0x60, 64
Configuration	F0,F1	0x370 (CFGEN bit in BSR register must be set.)
Real-Time Clock	F0,F1	0x70, 71 (CFGEN bit in BSR register must be cleared.)
GPR	F2	
GPW	F3	
Access.BUS	F4-F7	

Figure 24: IMSAI Super-I/O Board on-board Registers

	7	6	5	4	3	2	1	0
Mnemonic	CFGEN			BANK[4]	BANK[3]	BANK[2]	BANK[1]	BANK[0]
Reset	1	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 25: Bank Select Register, 80H (BSR)

BANK[4:0]: These bits select the current addressed bank of FLASH. Valid bank numbers range from 0 to 31. Bank 00h is selected upon RESET.

CFGEN: This bit allows software to access the FDC37C935APM configuration ports located at I/O address 0F0h-0F1h. When this bit is set, the FDC37C935APM can be put into configuration mode by writing 055h to I/O port 0F0h. Subsequent writes to I/O ports 0F0h and 0F1h are needed to configure the FDC37C935APM. When this bit is cleared, I/O accesses to port 0F0h and 0F1h access the Super I/O real-time clock registers instead of the configuration ports.

	7	6	5	4	3	2	1	0
Mnemonic						WSZ[2]	WSZ[1]	WSZ[0]
Reset	0	0	0	0	0	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 26: Window Size Register, 81H (WSR)

WSZ[2:0]: These bits select the Window Size for the FLASH according to the following table:

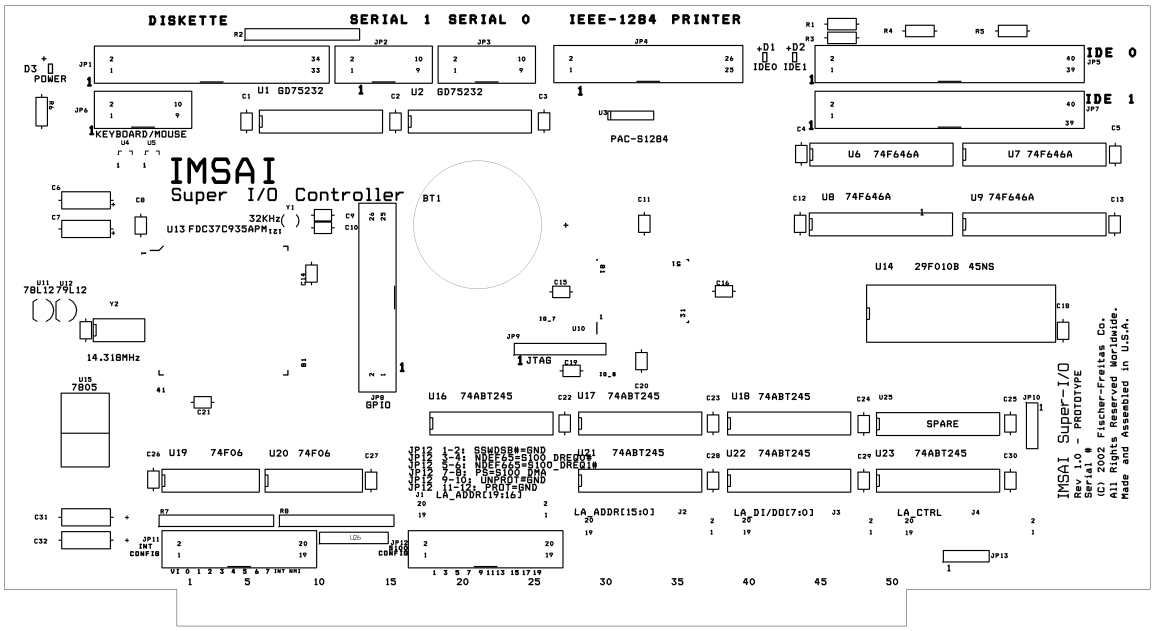
WSZ[2:0]	Window Size	# of Banks	
0	FLASH Disabled	0	
1	4K	32	
2	8K	16	
3	16K	8	
4	32K	4	
5	64K	2	
6	128K	1	

Figure 27: Window Size Selection Bit Definition

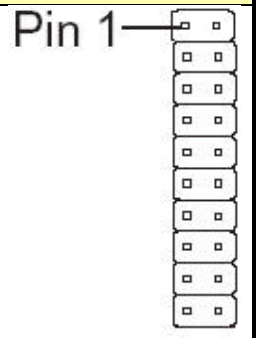
	7	6	5	4	3	2	1	0
Mnemonic	A19	A18	A17	A16	A15	A14	A13	A12
Reset	0	0	0	0	1	1	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 28: FLASH Base Address Register, 82H (BAR)

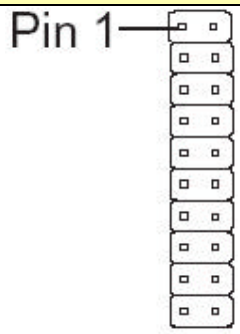
A[19:12]: These register selects the base address of the FLASH device in the memory map. When a 4K window size is selected, all address bits in the BAR must match the current memory cycle address in order for the FLASH to be selected. When a 128K window size is selected, only bits A[19:17] are compared.



Interrupt Configuration Jumper Block (JP11)

Jumper Block JP11	Description (When jumper is inserted)	Notes	
1-2	SMsC IRQ10 maps to IEEE-696 VI0	[DEFAULT]	
3-4	SMsC IRQ9 maps to IEEE-696 VI1	[DEFAULT]	
5-6	SMsC IRQ8 maps to IEEE-696 VI2	[DEFAULT]	
7-8	SMsC IRQ7 maps to IEEE-696 VI3	[DEFAULT]	
9-10	SMsC IRQ6 maps to IEEE-696 VI4	[DEFAULT]	
11-12	SMsC IRQ5 maps to IEEE-696 VI5	[DEFAULT]	
13-14	SMsC IRQ4 maps to IEEE-696 VI6	[DEFAULT]	
15-16	SMsC IRQ3 maps to IEEE-696 VI7	[DEFAULT]	
17-18	SMsC IRQ3 maps to IEEE-696 INT		
19-20	SMsC IRQ3 maps to IEEE-696 NMI		
Note: odd pins on Jumper block JP11 may be used as testpoints to their respective S-100 bus signals. Odd pins are connected to the S-100 bus, while even pins are connected to the Super I/O local bus.			

S-100 Bus Configuration Jumper Block (JP12)

Jumper Block JP12	Description (When jumper is inserted)	Notes	
1-2	S100 SSWDSB# tied to ground.	[DEFAULT]	
3-4	IEEE-696 NDEF65 is S100_DREQ0	[DEFAULT] (S2 Specific)	
5-6	IEEE-696 NDEF66 is S100_DREQ1	[DEFAULT] (S2 Specific)	
7-8	S100 PS is S100_DMA	[DEFAULT] (S2 Specific)	
7-9	L_DMA tied to gound.	Necessary when the Super I/O board is used in a system without DMA.	
9-10	UNPROT tied to ground.	[DEFAULT]	
11-12	PROT tied to ground	[DEFAULT]	
14	SS Test Point		
16	RUN Test Point		
18	RFU27 Test Point		
20	PINTE Test Point		
Note: even pins on Jumper block JP12 may be used as testpoints to their respective S-100 bus signals. Even pins are connected to the S-100 bus, while odd pins are connected to the Super I/O local bus.			

Super-I/O Controller Connector Pinouts

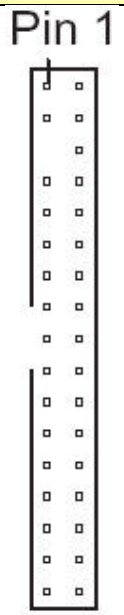
Signal	Description	Direction	2x17 Header Pin Number	
DRVDEN0		In	2	
N/C	No Connect		4	
DRVDEN1		In	6	
INDEX#	index pulse	In	8	
MTR_EN0#	Motor 0 Enable	Out	10	
DRVSEL0#	Drive Select 0	Out	12	
DRVSEL1#	Drive Select 1	Out	14	
MTR_EN1#	Motor 1 Enable	Out	16	
DIR#	Step Direction	Out	18	
STEP#	Step Pulse	Out	20	
WDATA#	Write Data	Out	22	
WGATE#	Write Gate	Out	24	
TRACK0#	Track 0 signal	In	26	
WPROT#	Write Protect	In	28	
MEDIA_ID0	Media ID bit 0	In	29	
RDATA#	Read Data	In	30	
HDSEL#	Head Select	Out	32	
MEDIA_ID1	Media ID bit 1	In	33	
DSK_CHG#	Disk Change	In	34	
GND	Ground	-	Unlisted pins	

Figure 29: JP1 - Super-I/O Floppy Drive Connector

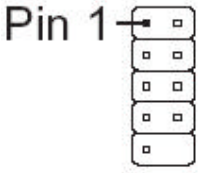
Signal	Description	Direction	MPU-C 2x5 Header Pin Number	DB9-M Connector on Cabinet	DB25-M Connector on Cabinet	
DCD	Data Carrier Detect	In	1	1	8	
DSR	Data Set Ready	In	2	6	6	
RxD	Receive Data	In	3	2	3	
RTS	Request to Send	Out	4	7	4	
TxD	Transmit Data	Out	5	3	2	
CTS	Clear to Send	In	6	8	5	
DTR	Data Terminal Ready	Out	7	4	20	
RI	Ring Indicator	In	8	9	22	
GND	Signal Ground	-	9	5	7	
-	Key	-	10	-	-	

Figure 30: JP2, JP3 - Super-I/O Serial Ports 0 and 1.

Signal	Description	Direction	MPU-C 2x5 Header Pin Number	DB25-F Connector on Cabinet	Centronics 36Pin	
STROBE#	Strobe Signal	Out	1	1	1	
AUTOFD#	Auto Linefeed	Out	2	14	14	
DATA0	Data Line 0	I/O	3	2	2	
ERROR#	Error	In	4	15	32	
DATA1	Data Line 1	I/O	5	3	3	
INIT	Initiate Output	Out	6	16	31	
DATA2	Data Line 2	I/O	7	4	4	
SELECTIN#	Printer Select	Out	8	17	36	
DATA3	Data Line 3	I/O	9	5	5	
GND	Signal Ground	-	10	18	16	
DATA4	Data Line 4	I/O	11	6	6	
GND	Signal Ground	-	12	19	17	
DATA5	Data Line 5	I/O	13	7	7	
GND	Signal Ground	-	14	20	19	
DATA6	Data Line 6	I/O	15	8	8	
GND	Signal Ground	-	16	21	20	
DATA7	Data Line 7	I/O	17	9	9	
GND	Signal Ground	-	18	22	21	
ACK#	Acknowledge	In	19	10	10	
GND	Signal Ground	-	20	23	22	
BUSY	Busy	In	21	11	11	
GND	Signal Ground	-	22	24	23	
PE	Paper Error	In	23	12	12	
GND	Signal Ground	-	24	25	24	
SELECT	Printer Selected	In	25	13	13	
-	Key	-	26	-	-	
GND	Signal Ground	-	-	-	25	
GND	Signal Ground	-	-	-	26	
GND	Signal Ground	-	-	-	27	
GND	Signal Ground	-	-	-	28	
GND	Signal Ground	-	-	-	28	
GND	Signal Ground	-	-	-	29	
GND	Signal Ground	-	-	-	30	
GND	Signal Ground	-	-	-	33	

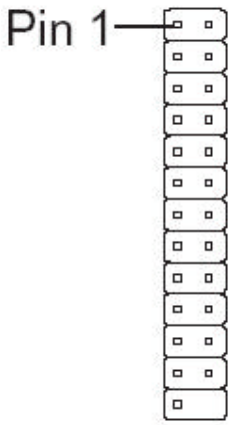


Figure 31: JP4 - Super-I/O Parallel Port

Signal	Description	Direction	2x20 Header Pin Number		
RESET*	Reset HD	Out	1		
GND	Ground	-	2		
HD7	HD data 7	In/Out	3		
HD8	HD data 8	In/Out	4		
HD6	HD data 6	In/Out	5		
HD9	HD data 9	In/Out	6		
HD5	HD data 5	In/Out	7		
HD10	HD data 10	In/Out	8		
HD4	HD data 4	In/Out	9		
HD11	HD data 11	In/Out	10		
HD3	HD data 3	In/Out	11		
HD12	HD data 12	In/Out	12		
HD2	HD data 2	In/Out	13		
HD13	HD data 13	In/Out	14		
HD1	HD data 1	In/Out	15		
HD14	HD data 14	In/Out	16		
HD0	HD data 0	In/Out	17		
HD15	HD data 15	In/Out	18		
GND	Ground	-	19		
N/C	No Connect	-	20		
AEN	Address Enable	Out	21		
GND	Ground	-	22		
IOW*	I/O Write	Out	23		
GND	Ground	-	24		
IOR*	I/O Read	Out	25		
GND	Ground	-	26		
IOCHRDY	I/O Channel Ready	In	27		
BALE	Bus Address Latch Enable	Out	28		
N/C	No Connect	-	29		
GND	Ground	-	30		
IRQ	Interrupt Request	In	31		
IOCS16*	16 bit transfer	In	32		
A1	Address 1	Out	33		
GND	Ground	-	34		
A0	Address 0	Out	35		
A2	Address 2	Out	36		
HCS0*	HD Select 0	Out	37		
HCS1*	HD Select 1	Out	38		
LED	HDD activity LED (-)	In	39		
GND	Ground	-	40		

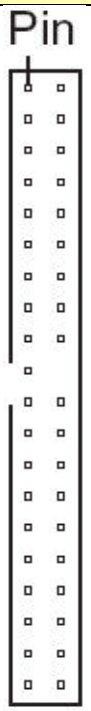


Figure 32: JP5,7 - Super-I/O IDE Channel 0 and 1 Connectors

Signal	Description	Direction	MPU-C 2x5 Header Pin Number		6-Pin Female Mini-DIN on Chassis	
-	No Connect	-	1		-	
KDATA	Keyboard Data	I/O	2		1	
KCLK	Keyboard Clock	O	3		5	
-	Key	-	4		2,6	
KGND	Keyboard Ground	O	5		3	
-	No Connect	-	6		-	
MDATA	Mouse Data	I/O	7		1	
MCLK	Mouse Clock	O	8		5	
-	No Connect	-	9		2,6	
MGND	Mouse Ground	-	10		3	

Figure 33: JP6 - Super-I/O PS/2 Keyboard/Mouse Port

Signal	Description	Direction	13x2 Header Pin Number		
GPIO10	SMsC GPIO 10	In/Out	1		
GPIO11	SMsC GPIO 11	In/Out	2		
GPIO12	SMsC GPIO 12	In/Out	3		
GPIO13	SMsC GPIO 13	In/Out	4		
GPIO14	SMsC GPIO 14	In/Out	5		
GPIO15	SMsC GPIO 15	In/Out	6		
GPIO16	SMsC GPIO 16	In/Out	7		
GPIO17	SMsC GPIO 17	In/Out	8		
GPIO20	SMsC GPIO 20	In/Out	9		
GPIO21	SMsC GPIO 21	In/Out	10		
GPIO22	SMsC GPIO 22	In/Out	11		
GPIO23	SMsC GPIO 23	In/Out	12		
GPIO24	SMsC GPIO 24	In/Out	13		
GPIO25	SMsC GPIO 25	In/Out	14		
GPIO60	SMsC GPIO 60	In/Out	15		
GPIO61	SMsC GPIO 61	In/Out	16		
GPIO62	SMsC GPIO 62	In/Out	17		
GPIO63	SMsC GPIO 63	In/Out	18		
GPIO64	SMsC GPIO 64	In/Out	19		
GPIO65	SMsC GPIO 65	In/Out	20		
GPIO66	SMsC GPIO 66	In/Out	21		
GPIO67	SMsC GPIO 67	In/Out	22		
GPIO53	SMsC GPIO 53	In/Out	23		
GPIO54	SMsC GPIO 54	In/Out	24		
GND	Ground	-	25		
GND	Ground	-	26		

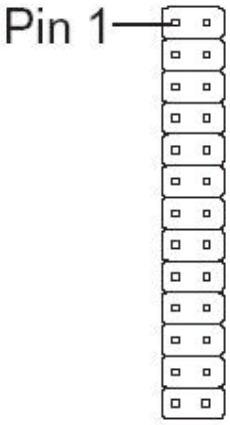


Figure 34: JP8 - Super-I/O GPIO Header Pinout

Please note: The GPIO pins provided on the IMSAI Super I/O Controller are directly connected to the SMsC Super I/O controller. They are not buffered and have no additional protection, so extreme caution should be used when using these pins. These pins can sink only 4mA and source only 2mA.

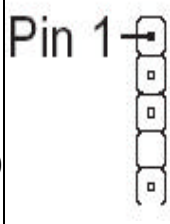
Signal	Description	Direction	1x8 Header Pin Number		
TRST#	Test Mode Reset	In	1	See Lattice Semiconductor M4A5 Datasheet for more information. (http://www.latticesemi.com)	
TDO	JTAG Data Out	Out	2		
TDI	JTAG Data In	In	3		
ENABLE#	Enable	In	4		
-	Key	-	5		
TMS	Test Mode Select	In	6		
GND	Signal Ground	-	7		
TCK	JTAG Clock	In	8		

Figure 35: JP9 - Super-I/O ISP Download Port

3. References

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4.82C59A CMOS Priority Interrupt Controller Datasheet, Intersil Corporation, March, 1997.

5.AT29C256 5-Volt Only FLASH Memory Datasheet, Atmel Corporation, 1999.

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7.CP/M 3.0 System Guide, Digital Research, 1983.

8. Technical Reference, Personal Computer AT, International Business Machines Corporation, September, 1985. (6139362)